



High Speed Counter Modules with PLS Outputs

Delivery Code 3DAY

EZIO System supports two High Speed 24 bit Counter Modules with PLS outputs that accept quadrature encoder inputs. The PLS outputs compare the counter value to two on/off presets and turn on outputs within 100µs of position change. Presets can be loaded into the counter modules from EZPLC. All inputs and outputs are optically isolated. In addition, PLS outputs are 0.5A short circuit proof DC outputs.

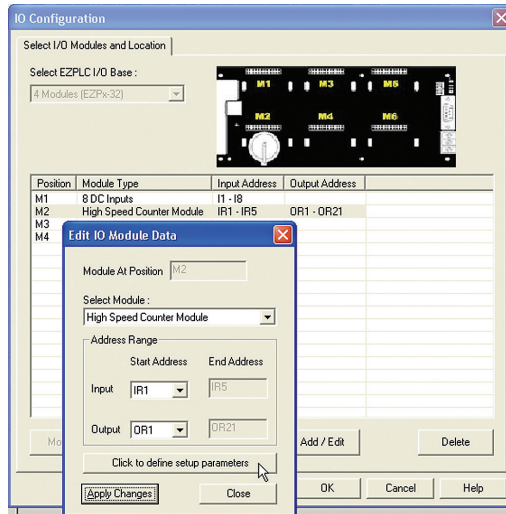
The counters have various preset/reset and inhibit modes as shown on the following page.



**EZIO-HSCM1
EZIO-HSCM2
Screw-down**

Configuring your High Speed Counter Module is EZier than Ever!

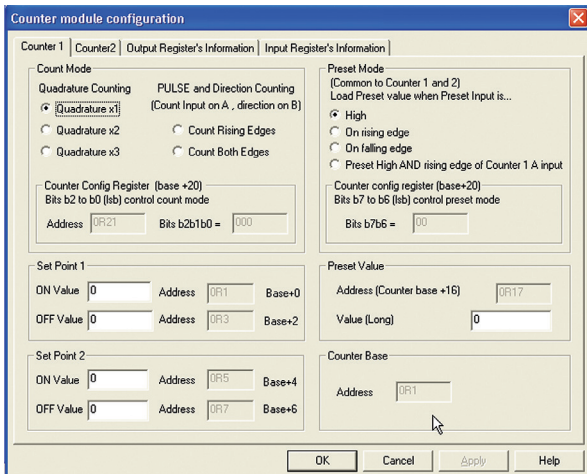
1 In EZPLC's I/O configuration specify the range of registers to be used for input and output.



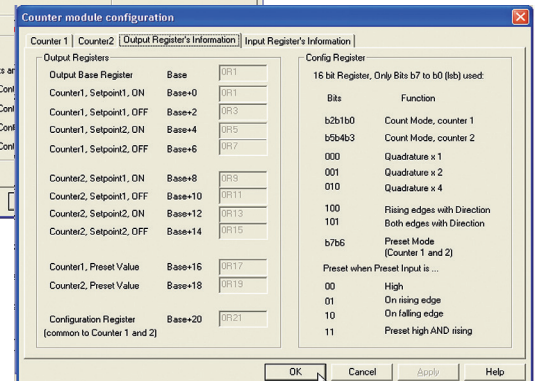
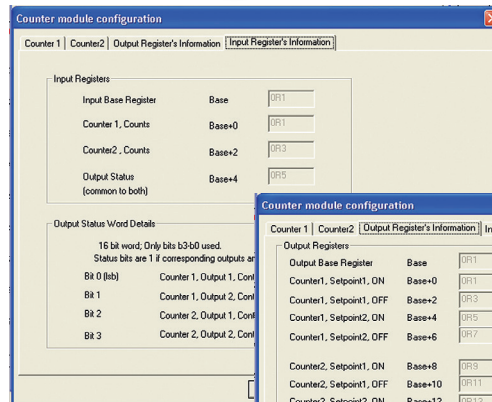
2 Counter Pin Out	
Pin No.	EZIO-HSCM1 (dual counter)
1	Quad A encoder 1
2	Quad B encoder 1
3	Quad A encoder 2
4	Quad B encoder 2
5	Common
6	Preset
7	Counter 1 Output 1
8	Counter 1 Output 2
9	Counter 2 Output 1
10	Counter 2 Output 2
11	Vs+

1 Counter Pin Out	
Pin No.	EZIO-HSCM2 (single counter)
1	Quad A encoder 1
2	Quad B encoder 1
3	Inhibit
4	Reset
5	Common
6	Preset
7	Counter 1 Output 1
8	Counter 1 Output 2
9	Counter 1 Output 3
10	Counter 1 Output 4
11	Vs+

2 Configure pulse, direction, quadrature counting, set points, preset values and preset mode



3 Detailed information for input and output registers





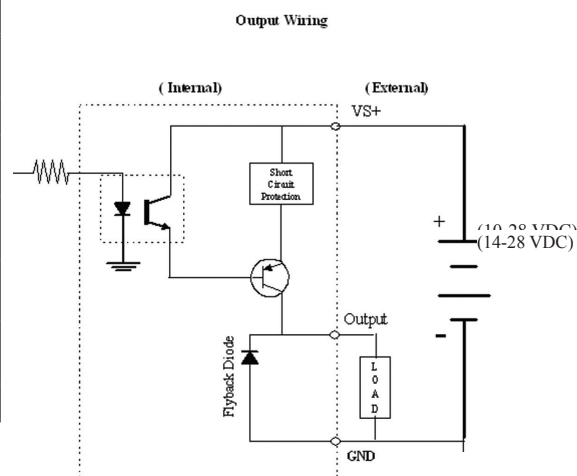
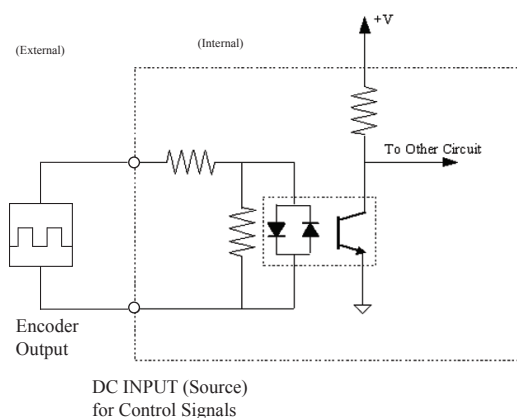
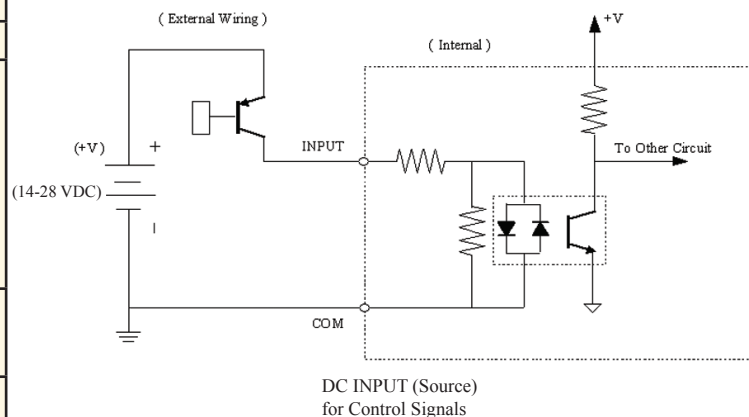
High Speed Counter Module Specifications

Module Specifications		
Feature	EZIO-HSCM1 (dual)	EZIO-HSCM2 (single)
Module Type	Intelligent High Speed Dual Counter Module	Intelligent High Speed Single Counter Module
Maximum Input Frequency	100KHz after 1X, 2X or 4X Multiplication	60KHz after 1X, 2X or 4X Multiplication
Minimum Pulse Width	5 μ s	
Resource Options	1X, 2X, or 4X Quadrature, Up or Down Counter, Reset	
Counter Range	16 million (24 bits)	
Preset Modes	<ol style="list-style-type: none"> This mode will preset the counter to the preset value while preset is held high. While the preset signal is high, no new count signals will be counted. This mode will create an interrupt on the rising edge of the reset signal to set the counter to the preset value. This mode will create an interrupt on the falling edge of the preset signal to set the counter to the preset value. This mode will create a preset pulse every time that there is a rising edge of signal A and the preset signal is high. 	
Reset Modes/Input	None	Same as Preset except the reset input sets the counter value to zero
Inhibit Input	None	Inhibits the counter from counting when high

PLS Output Specifications		
Feature	EZIO-HSCM1 (dual counter)	EZIO-HSCM2 (single counter)
Number of Outputs	2 Source outputs for each counter	4 Source outputs
Response Time	100 μ s	
PLS Setpoints	1 on/off pair for each output	
Peak Voltage	50.0 VDC	
Maximum Steady State Output Current	0.5A per output, 1.0A max per module @ 50°C	
Maximum Leakage Current	100 μ A @ 50 VDC @ 50°C	
ON Voltage Drop	2 VDC @ 0.5A	
Maximum Inrush Current	0.8A for 10ms	
OFF to ON Response	< 2 μ s	
ON to OFF Response	<10 μ s	
Status Indicators	Red LED for each output	
+V Terminals & Commons	One V*, 1 Common	
Short Circuit Protection	1 Amp per module, turns off outputs upon short circuit detection	
Optical Isolation	2500 Volt	

Counter Input Specifications		
Feature	EZIO-HSCM1 (dual counter)	EZIO-HSCM2 (single counter)
Number of Inputs	5	
Input Voltage Range	14-28 VDC	
Peak Voltage	40 VDC	
Input Current	2.5 mA @ 14 VDC 5.0 mA @ 28 VDC	
Maximum Input Current	5 mA @ 28 VDC	
Input Impedance	5.6K Ω min. @ 14-28 VDC	
ON Voltage Level	> 14 VDC	
OFF Voltage Level	< 2 VDC	
Min. ON Current	2.5 mA	
Min. OFF Current	0.2 mA	
OFF to ON Response	< 2 μ s	
ON to OFF Response	< 3 μ s	
Status Indicators	Red LED for each input	
Commons	1 point	

General Specifications	
Optical Isolation	2500 Volt
Wires	1 of 14 AWG, 2 of 18 AWG, 4 of 22 AWG
Operating Environment	0-60°C, Humidity non-condensing 5-95%



For EZ-LINK cables and Terminal boards look at page 4-5